PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : H05K 3/46, 3/00, 1/00 — A1

(11) International Publication Number: WO 00/25558

(43) International Publication Date: 4 May 2000 (04.05.00)

(21) International Application Number: PCT/SE99/01930

(22) International Filing Date: 26 October 1999 (26.10.99)

(30) Priority Data:
9803671-8 26 October 1998 (26.10.98) SE

(71) Applicant: TELEFONAKTIEBOLAGET LM ERICSSON [SE/SE]; S-126 25 Stockholm (SE).

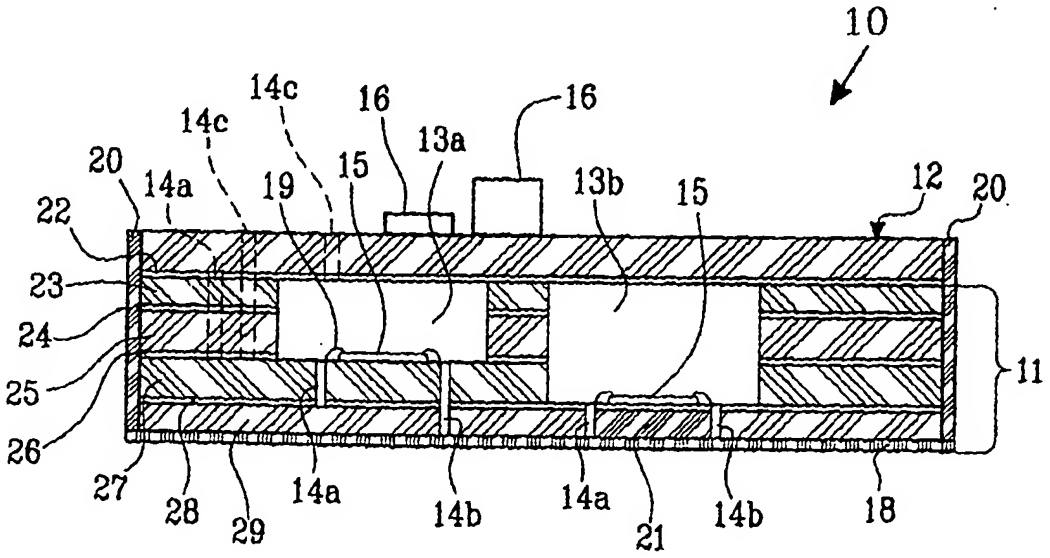
(72) Inventor: SÖDERHOLM, Mats; Apelvägen 10, S-430 33 Fjärås (SE).

(74) Agent: GÖTEBORGS PATENTBYRÅ DAHLS AB; Sjöporten 4, S-417 64 Göteborg (SE).

(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: A CIRCUIT BOARD AND A METHOD FOR MANUFACTURING THE SAME



(57) Abstract

The present invention refers to a circuit board (10), in particular a multilayer circuit board including at least a first carrying section (11) and a second section (12), conductor pattern (17a, 17b, 17c) and via holes (14, 14b, 14c), at least one of the sections (11; 12) comprises at least one cavity (13a, 13b) for receiving at least one electric component (15), preferably a naked circuit, the second section (11; 12) constitutes a protective cover essentially hermetical sealing of the component (15). The circuit board (10) comprises substrates of a non ceramic material and that said substrates are protected against moisture penetrating in the transverse direction of the substrates by means sealing arranged at outer edges of the substrates.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece			TR	Turkey
BG	Bulgaria	HU	Hungary	ML	Mali	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MN	Mongolia	UA	Ukraine
BR	Brazil	IL	Israel	MR	Mauritania	UG	Uganda
BY	Belarus	IS	Iceland	MW	Malawi	US	United States of America
CA	Canada	IT	Italy	MX	Mexico	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NE	Niger	VN	Viet Nam
CG	Congo	KE	Kenya	NL	Netherlands	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NO	Norway	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	NZ	New Zealand		
CM	Cameroon			PL	Poland		
CN	China	KR	Republic of Korea	PT	Portugal		
CU	Cuba	KZ	Kazakstan	RO	Romania		
CZ	Czech Republic	LC	Saint Lucia	RU	Russian Federation		
DE	Germany	LI	Liechtenstein	SD	Sudan		
DK	Denmark	LK	Sri Lanka	SE	Sweden		
EE	Estonia	LR	Liberia	SG	Singapore		

Title

A CIRCUIT BOARD AND A METHOD FOR MANUFACTURING THE SAME

TECHNICAL FIELD

The present invention relates to a circuit board, in particular a multilayer circuit board of the type, which comprises at least a first carrying board section and a second board section and a conductor pattern and via holes.

The invention also refers to a method to produce the circuit board.

BACKGROUND OF THE INVENTION

To increase the number of components and circuits on a circuit board certain circuits can be mounted directly on the circuit board without protective housing. These so-called naked circuits are used frequently in special applications in exposed environments and must be protected against the surroundings, e.g. against moisture. The circuit is normally glued with silver glue, a process that can result in silver migration, which as a result of the moisture may become aggravated. Generally, they are provided with a protective cover of a material capable of being hardened, in particular the entire circuit board is covered with this material, which in addition can complicate fault-detecting and repair of the board.

In certain applications the naked circuits or chips can be packaged in a package containing both the circuit and a board. The drawback with this method is that the package requires an extra accommodation.

Prior art discloses only packaging of circuits for use within microwave applications on or under a circuit board. The circuits are then arranged with a protection of a cover or bottom.

U.S. 4,276,558 describes, for example, an active microwave amplifier, which is hermetical encased onto the back of a dielectric substrate, whose front is occupied by means for transmission/reception of signals. Hermetical sealing can occur when the circuit is provided

with a lid with the same thermal characteristics as the substrate.

U.S. 5,229,727 describes a microstrip to microstrip junction through a hermetical sealing on a ceramic board.

Moreover, U.S. 5,712,767 discloses a circuit element mounting structure comprising: a substrate having a pattern A of wirings therein; at least one cavity formed at a surface of the substrate; and a cap for covering the cavity therewith, characterized by the cap including a pattern B of wirings therein and a connection B for electrically connecting the pattern B of wirings to the pattern A of wirings, and the substrate including a connection A for electrically connecting the connection B to the pattern A of wirings. In accordance with the invention, it is now possible to mount circuit elements on a cap which had been a dead space in prior circuit, and hence also possible to mount circuit elements in higher density on a substrate including a cap zone.

The cavities according to this invention are covered by means of covering the cavity with metal and then a metallized lid is soldered to the metal cover. The lids are arranged as electrical screening. Accordingly, each cavity is covered with a metallic cover, which results in time and cost consuming sealing processes.

JP7022730 aims to reduce the occupying area in a composite electronic component including the combination of multilayer circuit boards and an electronic component chip. Therefore, a plurality of multilayer circuit boards having a cavity in which an electronic component chip is built are stacked in a condition of being mutually bonded to one other by a bonding agent. This enables the built-in electronic components to be discriminated between non-defective and defective at the pre-stacking stage of individual multilayer circuit boards.

The main object of this invention is to reduce the number of substrates carrying naked chips so if a chip is defective and the substrates must be discarded, not a few chips are discarded. To achieve an effective assembly, the substrates are stacked on each other and the naked chips are located inside the cavities of the stack. Neither hermetic sealing nor moisture barriers are considered as plastic substrates are used.

SUMMARY OF THE INVENTION

The object of the present invention is to produce a new type of circuit board, comprising substrates made of non ceramic material, which allows much larger density of components than what has been possible. Non ceramic materials are generally much cheaper than ceramic material.

A second object of the invention is to allow hermetical sealing and integration of electric components, in particular naked chips to the board.

A third object of the invention is to be able by using the non ceramic board material obtaining essentially hermetical sealing of components.

A further object of the present invention is to achieve isolation of sealed components, in particular against penetration of moisture in transversal direction.

An advantage with the board according to the invention is that it can be arranged in a cooling medium without damage to the components in the hermetical sealed cavities.

These objects are obtained through the initially mentioned circuit board, which in at least one of the board sections includes at least one cavity for placing of at least one electric component, preferably a naked circuit. The second board section constitutes a protective cover for essentially hermetical sealing of the component.

In one embodiment, the section arranged as cover at least partly covers the first section.

The component provided in the cavity can suitably be connected to other components in other layers through the via holes.

Depending on the applications and components that are used the board comprises different cavities with different volumes. The number of components that can be mounted can be increased the second section, arranged as a cover, which can be arranged to provide further

components.

To isolate the board against for instance penetration of moisture the edges of the sections are plated, which can be done before or after the assembly of the sections and a possible joint between the sections are adhered as moisture barrier.

Preferably one of the sections is provided with a groove while the other one is provided with corresponding elevation designed to, in cooperation with the grooves, provide a moisture barrier and/or assembly references.

In one embodiment the component in the cavity can be surface mounted.

To achieve same thermal expansion, the sections consist of a material with the same thermal characteristics, which can consist of woven glass fibre with adhesive of thermoplast. Suitably the adhesive contains ceramic filling.

The invention also comprises a method for manufacturing a circuit board, preferably a multilayer circuit board including at least a first carrying board section and a second board section and a conductor pattern and via holes. The method includes the primary steps of: producing laminate layers of a non ceramic material, producing via holes in the laminate layers, plating desired via holes, filling the via hole with a filler, providing a cavity in laminate layer, providing desired laminate layer with a conductor layer or pattern, joining together the laminate layers, filling the holes with the filler through screen printing, removing possible section of laminate functioning as cover, and arranging a moisture barrier on the edge of said laminates. The method also comprises the steps of plating the edges of the layers. According to the method the components are arranged in the cavity and a laminate layer is arranged so that it covers the cavity.

BRIEF DESCRIPTION OF THE DRAWINGS

In the following the invention will be described with reference to embodiments shown in the attached drawings, in which:

Fig. 1 is a schematic perspective view of a circuit board according to the invention, and
Fig. 2 is a schematic but more detailed cross section of the board according to fig.1 along line II-II.

DESCRIPTION OF ONE EMBODIMENT

The circuit board 10 shown in fig. 1 and 2 comprises a first substrate 11 which constitutes a first board section and a second substrate 12, which comprises a second board section, cavities 13a and 13b, via holes (through holes) 14a, 14b and 14c, sealed circuits 15, possible externally mounted circuits/components16 as well as conductor pattern 17a, 17b and 17c.

The via holes 14a and 14b refer to via holes that connect between cavities and upper/lower conductor layers, while the via holes 14c refers to via holes that connect the conductor layers of the first section 11 or the conductor layers between the first and the second section 12. The conductor pattern 17a refers to conductors in the first board section and in the cavities, 17b refers to conductors on the first board section (between the first and second board section) and 17c refers to conductors on the second board section. It should be noticed that the existence of conductor layers and via holes in different layers inside and on the substrates depend on the design of the circuit boards and not limited to the shown and illustrated embodiment. Furthermore the conductors are produced and connected between different layers in a way well-known to a skilled person.

Preferably, the section 12 is a conductor layer itself and can, depending on the application, consist of any desired material. However, it is suitable to use a material with the same thermal characteristics as section 11.

In a preferred embodiment the sections are made of a substrate or laminate provided with external conducting layers 18 of copper, so-called base copper. When no other components are mounted to the circuit board, the base copper can constitute the utmost layer, which however

can be arranged with further laminate layers. The electronics 15 are then arranged inside the board in the cavities 13a and 13b, which can have different volumes. The electronics 15 can be mounted, e.g. through surface mounting or other method. In case of surface mounting the electronics are adhered in position and bonded with bonding wires 19.

The section 11, which includes the cavities and the electronics is joined together with the second section 12, which constitutes a lid for the cavities 13a, 13b. The assembly can be done by adhesives such as glue, soldering or the like. Possibly, a mechanical assembly, e.g. screw joint may be provided. The board assembly is then provided with edge platings 20, preferably around the entire board. The board may also be edge plated, depending on its design, before the joining. The edge plating results in that the board becomes hermetical, e.g. against moisture. The seal between the boards can then be soldered or glued to further prevent passage of moisture through the seal between the boards. In an embodiment one of the board sections can be provided with grooves at the edges while the second one is provided with corresponding elevations, which in cooperation with the grooves are intended to constitute a moisture barrier and/or assembly references. The edge plating may substituted by a moisture barrier of plastic, rubber, PVC, an adhesive agent or the like.

If circuits which require cooling are used, the first board section 11 can at least partly be provided with metal carriers 21, which, e.g. can be laminated together with the rest of the board (besides the lid) and edge plated or assembled similar to the upper second board section 12. It appears from fig. 2 that cavities with different levels can be found. The cavity 13a can, e.g. be provided with laminate for wiring over the metal carrier for components that not need cooling, while the cavity 13b can be arranged directly or, e.g. through a rubber block in contact with the metal carrier. If no components are provided on the board, the entire board can be arranged in a cooling medium, such as water or the like without damage to the components.

According to fig. 2 the first board section 11 consists of a number of layers. At least parts of the surface of the board section are provided with a conducting pattern 22 (17b), constituting conductors, ground plane or the like. The pattern is plated to a laminate 23 of an insulating material. A layer of prepreg can be applied between the laminate layer 23 and the second conductor layer 24 arranged on a second laminate layer 25. Between the laminate layer 23 and

a conductor layer 26 a second layer of prepreg can be applied. The conductor layer 26 is arranged on a laminate layer 27, which, even on the underside, is provided with a conductor layer 28 and a laminate 29. The conductor layers are intended as, e.g. connections, ground plane and so on. Between the different layers surface treatment or adhesives can be applied, in particular between the prepreg-laminate or prepreg-conductor.

The cavities 13a, 13b are recesses which are produced during the manufacture of the board, e.g. by using layers with recesses corresponding to the form of the cavity. The cavities can be made, e.g. through milling, punching and so on. The conductor patterns in the cavities are applied during the fabrication, e.g. through plating. When using laminates provided with base copper the patterns are etched and plated by a suitable surface treatment. Obviously, other methods can be used. In order to prevent damaging the surface treatment the cavity within the layer structure is left with a "lid" in the final layer and a "bottom"intact. The lid is milled away when the board section is finished.

It should be noticed that the embodiment according to the figures is merely given as a non limiting example and configurations comprising other layouts and layer structures can occur.

The board can be manufactured through different methods. However a method is described in association with manufacturing of through holes in a pending Swedish patent application no. 9803670-0, by the same applicant.

Following non limiting example describes some important steps during manufacture of a circuit board, in accordance with the invention:

- a laminate layer 29 provided with base copper manufactured according to known technique;
- the laminate layer 29 is then provided with via holes 14;
- then desired via holes are plated;
- the holes are filled with a filler;
- a new laminate layer 27 is then manufactured;
- the first section of the cavity 13b is recessed;
- possibly the laminate layer is provided with a conductor layer or pattern;

- then the laminate layer 27 and 29 are joined together by means of prepreg;
- via holes 14 are then drilled and plated;
- the holes are filled with the filler through screen printing from the front and/or the back and are subsequently hardened;
- afterwards new laminate layers 23, 25 provided with recesses for the cavities 13a, 13b are provided;
- then all laminate layers are assembled (laminated together);
- conductor patterns are created;
- the via holes are then drilled and plated;
- possible section of the laminate functioning as "lid" is milled away;
- a final laminate layer12 is manufactured;
- the boards are provided with edge plating, and
- the sections are assembled after installation of the components in the cavities.

Obviously, one or more of the above described stages can be performed in parallel as well as in a different order.

Preferably, the filler is left in the holes, for instance to achieve hermetical sealing. However, the fillings can be removed at any area in a suitable way.

The substrates consist of an appropriate non ceramic material, preferably woven glass fibre with an adhesive of ceramic filled thermoplast or just thermoplast. Furthered, preferred materials are AROL 25N, AROL 25SR, ROGERS 4003, ROGERS 4350, cyanide esters, SR 4 and variants thereof. Additionally, base copper can be substituted with another conductive material, e.g. gold, silver or the like. The entire external surface of the board can also be provided with a layer, e.g. of copper.

The circuit board can be used within different applications within electronics, suitably it can be used as carrier in microstripsantennas or the like.

While we have illustrated and described a preferred embodiment of the invention, it is realized that many variations and modifications within the scope of the attached claims can be found.

CLAIMS

1. A circuit board (10), in particular a multilayer circuit board including at least a first carrying section (11) and a second section (12), conductor pattern (17a, 17b, 17c) and via holes (14, 14b, 14c), at least one of the sections (11; 12) comprises at least one cavity (13a, 13b) for receiving a least one electric component (15), preferably a naked circuit, the second section (11; 12) constitutes a protective cover essentially hermetical sealing of the component (15),
characterized in,
that the circuit board (10) comprises substrates of a non ceramic material and that said substrates are protected against moisture penetrating in the transverse direction of the substrates by means sealing arranged at outer edges of the substrates.

2. Circuit board according to claim 1,
characterized in,
that the section arranged as a cover at least partly covers the first section.

3. Circuit board according to claim 1,
characterized in,
that the component (15) provided in the cavity are connected to the other components (15, 16) in other layers by means of via holes (14, 14b, 14c).

4. Circuit board according to one of the claims 1- 3,
characterized in,
that the board includes different cavities (13a, 13b) with different volumes.

5. Circuit board according to any of the preceding claims,
characterized in,
that the second section arranged as cover is arranged to carry further components (16).

6. Circuit board according to any of the preceding claims,
characterized in,
that said edge sealing comprises edge plating (21).

7. Circuit board according to claim 6,
characterized in,
that the edge plating (21) is arranged before or after the assembly of the sections (11, 12).

8. Circuit board according to any of claims 1-5,
characterized in,
that said edge sealing comprises a moisture barrier of one of plastic, rubber, PVC or an adhesive agent.

9. Circuit board according to any of the preceding claims,
characterized in,
that a possible joint between the sections is adhered as a moisture barrier.

10. Circuit board according to any of the preceding claims,
characterized in,
that one of the sections is provided with a groove while the other is provided with a corresponding elevation, which in cooperation with the grooves, constitute a moisture barrier and/or mounting references.

11. Circuit board according to claim 1,
characterized in,
that the component (15) is surface mounted.

12. Circuit board according to any of the preceding claims,
characterized in,
that the sections (11, 12) are of a material with same thermal characteristics.

13. Circuit board according to claim 12,
characterized in,
that the material consists of woven glass fibre with an adhesive of thermoplast.

14. Circuit board according to claim 13,
characterized in,
that the adhesive includes ceramic filling.

15. Circuit board according to claim 11,
characterized in,
that furthered preferred substrates materials are one of AROL 25N, AROL 25SR, ROGERS 4003, ROGERS 4350, cyanide esters, SR 4 and variants thereof.

16. A method for manufacturing a circuit board, preferably a multilayer circuit board including at least a first carrying section (11) and a second section (12), conductor pattern (17a, 17b, 17c) and via holes (14, 14b, 14c),
characterized in,
that the method primarily includes the steps of:

- producing laminate layers (12, 23 35, 27, 29) of a non ceramic material,
- producing via holes (14) in the laminate layers (23, 35, 27, 29),
- plating desired via holes,
- filling the via hole with a filler,
- providing a cavity (13a, 13b) in laminate layer (23, 35, 27, 29),
- providing desired laminate layer with a conductor layer or pattern,
- joining together the laminate layers,
- filling the holes with the filler through screen printing,
- removing possible section of laminate functioning as cover, and
- arranging a moisture barrier on an edge of said laminates.

17. Method according to claim 16,
characterized in,
that it further includes the step of plating the edge of the layers.

18. Method according to any of the claims 16 or 17,
characterized in,
that it further includes the steps of arranging the components in the cavity and to adhere a

laminate layer to cover the cavity.

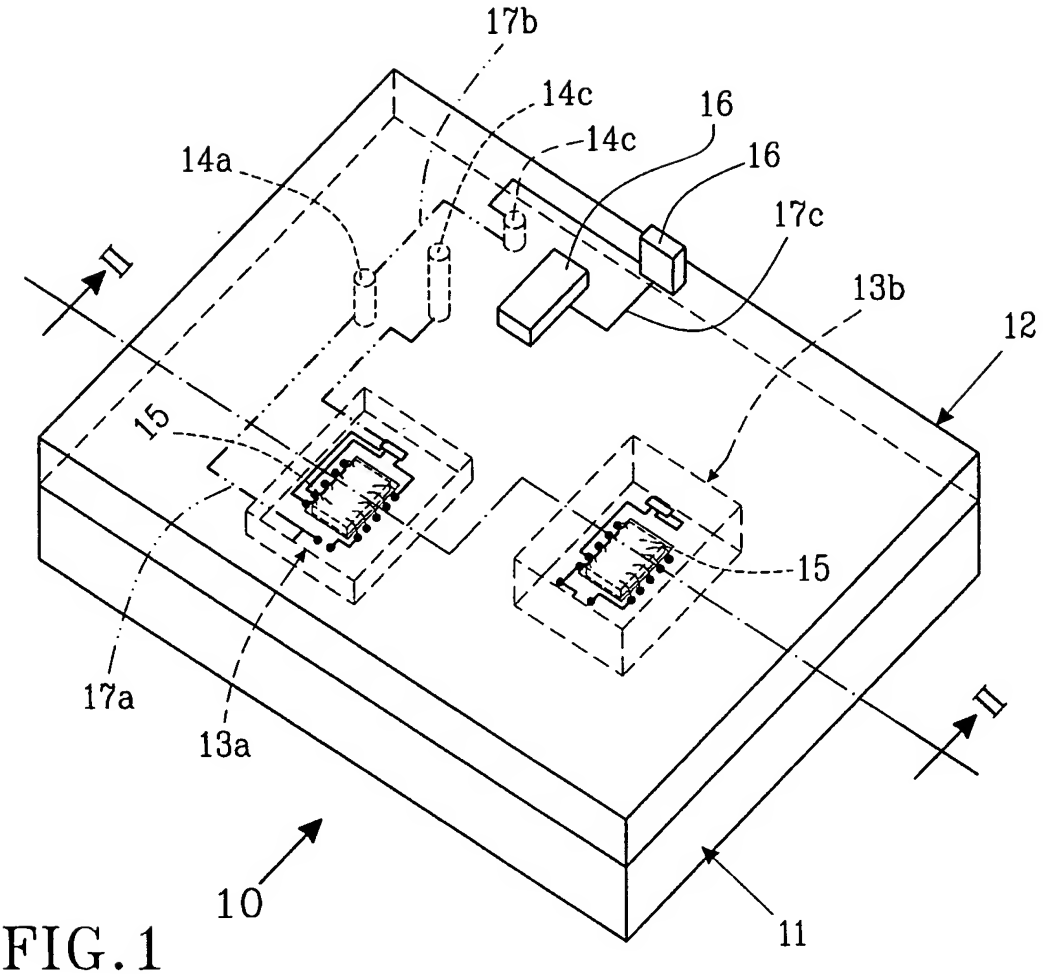

17b
14c
14c
16
16
14a
17c
13b
12
II
15
15
17a
13a
II
10
11

FIG.1

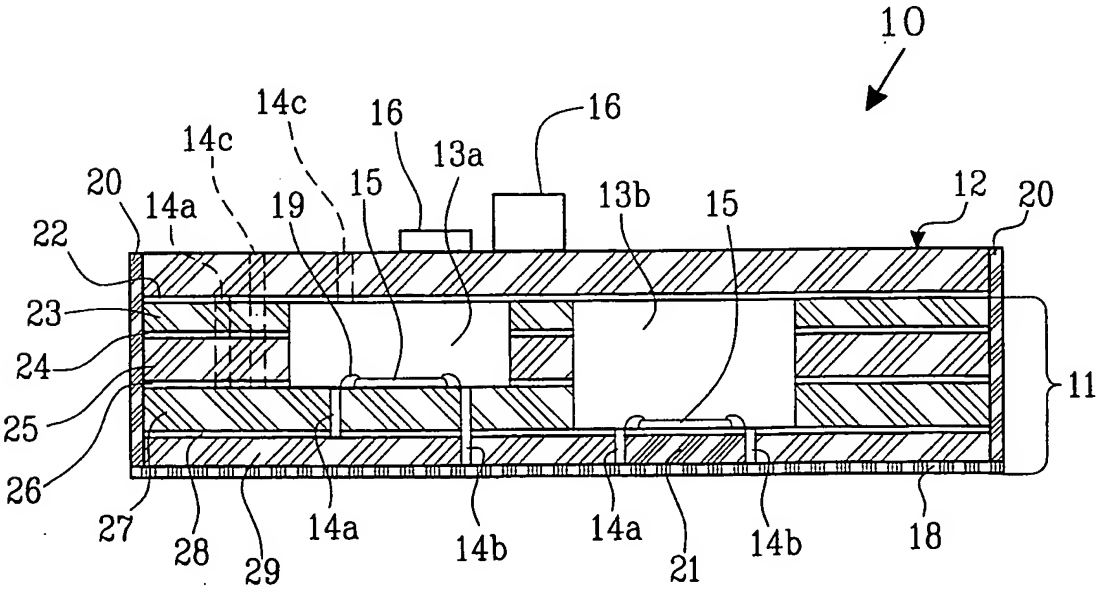

10
14c
14c
16
16
13a
20
14a
19
15
13b
15
12
20
22
23
24
25
26
11
27
28
29
14a
14b
14a
21
14b
18

FIG.2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 99/01930

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: H05K 3/46, H05K 3/00, H05K 1/00
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: H05K, H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPODOC, WPI, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5712767 A (TAKAO KOIZUMI), 27 January 1998 (27.01.98), column 3, line 36 - line 60, figures 5, 7,9 --	1-18
A	JP 7022730 A (MURATA MFG CO LTD) 1995-01-24 (abstract) World Patents Index (online). London, U.K.: Derwent Publications, Ltd. (retrieved on 1999-07-02). retrieved from : EPO WPI Database. DW9513, Accession No. 95-095690; & JP 7022730 (MURATA MFG CO LTD) 1995-05-31 (abstract). (online)(retrieved on 1999-07-02) Retrieved from: EPO PAJ Database. --	1-18
A	US 4276558 A (PANG T. HO ET AL), 30 June 1981 (30.06.81) --	1-18

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" erlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
8 March 2000	10 -03- 2000
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Bertil Dahl/ELY Telephone No. +46 8 782 25 00

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 99/01930

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5229727 A (RICHARD D. CLARK ET AL), 20 July 1993 (20.07.93) -- --------	1-18

INTERNATIONAL SEARCH REPORT

Information on patent family members

02/12/99

International application No.
PCT/SE 99/01930

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5712767 A	27/01/98	AU 699516 B	03/12/98
		AU 3787695 A	23/05/96
		CA 2161569 A	17/05/96
		CN 1133498 A	16/10/96
		EP 0713252 A	22/05/96
		JP 2682477 B	26/11/97
		JP 8148800 A	07/06/96
US 4276558 A	30/06/81	NONE	
US 5229727 A	20/07/93	NONE	